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\* Design Summary \*

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Top Level Output File Name : ALU.ngc

Primitive and Black Box Usage:

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# BELS : 598

# GND : 1

# LUT2 : 96

# LUT3 : 65

# LUT4 : 64

# LUT5 : 2

# LUT6 : 170

# MUXCY : 103

# MUXF7 : 32

# VCC : 1

# XORCY : 64

# FlipFlops/Latches : 33

# FD : 33

# Clock Buffers : 1

# BUFGP : 1

# IO Buffers : 101

# IBUF : 68

# OBUF : 33

Device utilization summary:

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Selected Device : 6slx9tqg144-3

Slice Logic Utilization:

Number of Slice Registers: 32 out of 11440 0%

Number of Slice LUTs: 397 out of 5720 6%

Number used as Logic: 397 out of 5720 6%

Slice Logic Distribution:

Number of LUT Flip Flop pairs used: 397

Number with an unused Flip Flop: 365 out of 397 91%

Number with an unused LUT: 0 out of 397 0%

Number of fully used LUT-FF pairs: 32 out of 397 8%

Number of unique control sets: 1

IO Utilization:

Number of IOs: 102

Number of bonded IOBs: 102 out of 102 100%

IOB Flip Flops/Latches: 1

Specific Feature Utilization:

Number of BUFG/BUFGCTRLs: 1 out of 16 6%

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Partition Resource Summary:

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No Partitions were found in this design.

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Timing Report

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

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Clock Signal | Clock buffer(FF name) | Load |

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clk | BUFGP | 33 |

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Asynchronous Control Signals Information:

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No asynchronous control signals found in this design

Timing Summary:

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Speed Grade: -3

Minimum period: 1.371ns (Maximum Frequency: 729.262MHz)

Minimum input arrival time before clock: 9.099ns

Maximum output required time after clock: 3.634ns

Maximum combinational path delay: No path found

Timing Details:

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All values displayed in nanoseconds (ns)

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Timing constraint: Default period analysis for Clock 'clk'

Clock period: 1.371ns (frequency: 729.262MHz)

Total number of paths / destination ports: 32 / 32

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Delay: 1.371ns (Levels of Logic = 1)

Source: result\_0 (FF)

Destination: result\_0 (FF)

Source Clock: clk rising

Destination Clock: clk rising

Data Path: result\_0 to result\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FD:C->Q 2 0.447 0.617 result\_0 (result\_0)

LUT6:I5->O 1 0.205 0.000 operation[3]\_in1[31]\_select\_19\_OUT<0>6 (operation[3]\_in1[31]\_select\_19\_OUT<0>)

FD:D 0.102 result\_0

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Total 1.371ns (0.754ns logic, 0.617ns route)

(55.0% logic, 45.0% route)

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Timing constraint: Default OFFSET IN BEFORE for Clock 'clk'

Total number of paths / destination ports: 36480 / 33

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Offset: 9.099ns (Levels of Logic = 23)

Source: in2<0> (PAD)

Destination: result\_0 (FF)

Destination Clock: clk rising

Data Path: in2<0> to result\_0

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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IBUF:I->O 12 1.222 1.156 in2\_0\_IBUF (in2\_0\_IBUF)

LUT4:I0->O 1 0.203 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_lut<0> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_lut<0>)

MUXCY:S->O 1 0.172 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<0> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<0>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<1> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<1>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<2> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<2>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<3> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<3>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<4> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<4>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<5> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<5>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<6> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<6>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<7> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<7>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<8> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<8>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<9> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<9>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<10> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<10>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<11> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<11>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<12> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<12>)

MUXCY:CI->O 1 0.019 0.000 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<13> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<13>)

MUXCY:CI->O 1 0.213 0.684 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<14> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<14>)

LUT5:I3->O 3 0.203 0.651 Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<15> (Mcompar\_in1[31]\_in2[31]\_LessThan\_9\_o\_cy<15>)

LUT4:I3->O 32 0.205 1.636 operation[3]\_in1[31]\_select\_19\_OUT<0>3211 (operation[3]\_in1[31]\_select\_19\_OUT<0>321)

LUT6:I1->O 2 0.203 0.981 operation[3]\_in1[31]\_select\_19\_OUT<0>2 (operation[3]\_in1[31]\_select\_19\_OUT<0>3)

LUT6:I0->O 1 0.203 0.000 operation[3]\_in1[31]\_select\_19\_OUT<0>5\_SW0\_F (N100)

MUXF7:I0->O 1 0.131 0.684 operation[3]\_in1[31]\_select\_19\_OUT<0>5\_SW0 (N4)

LUT6:I4->O 1 0.203 0.000 operation[3]\_in1[31]\_select\_19\_OUT<0>6 (operation[3]\_in1[31]\_select\_19\_OUT<0>)

FD:D 0.102 result\_0

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Total 9.099ns (3.307ns logic, 5.792ns route)

(36.3% logic, 63.7% route)

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Timing constraint: Default OFFSET OUT AFTER for Clock 'clk'

Total number of paths / destination ports: 33 / 33

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Offset: 3.634ns (Levels of Logic = 1)

Source: result\_31 (FF)

Destination: result<31> (PAD)

Source Clock: clk rising

Data Path: result\_31 to result<31>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

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FD:C->Q 2 0.447 0.616 result\_31 (result\_31)

OBUF:I->O 2.571 result\_31\_OBUF (result<31>)

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Total 3.634ns (3.018ns logic, 0.616ns route)

(83.0% logic, 17.0% route)

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Cross Clock Domains Report:

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Clock to Setup on destination clock clk

---------------+---------+---------+---------+---------+

| Src:Rise| Src:Fall| Src:Rise| Src:Fall|

Source Clock |Dest:Rise|Dest:Rise|Dest:Fall|Dest:Fall|

---------------+---------+---------+---------+---------+

clk | 1.371| | | |

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Total REAL time to Xst completion: 5.00 secs

Total CPU time to Xst completion: 4.97 secs

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Total memory usage is 4507976 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 0 ( 0 filtered)

Number of infos : 0 ( 0 filtered)